

Tofic David Esses

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Education

University of California, Berkeley

Aug 2025 - May 2026

Master of Engineering in Electrical Engineering and Computer Science, GPA: 3.75/4.0

- Courses: F25: Digital Design and Integrated Circuits, ASIC Lab, Analog Integrated Circuits, PCB Engineering
S26: Advanced Digital Integrated Circuits, Graduate Computer Architecture

McGill University

Sep 2020 – Dec 2024

Bachelor of Engineering in Electrical Engineering, GPA: 3.75/4.0

Montreal, Canada

- Courses: Machine Learning, Microprocessors, Microelectronics, Computer Vision, Embedded Systems

Technical Skills

Programming: Verilog, C, C++, Java, Python, RISC-V Assembly, Bash

ASIC / VLSI: Cadence Genus, Innovus, Virtuoso, VCS, SPICE, Assertions, RTL Design, Static Timing Analysis

Hardware Design: KiCad, Altium Designer, LTSpice, Schematic Capture, PCB Routing, Bring-up, SPI/I2C/UART

Integrated Circuits Projects

Gigabit Ethernet PHY | Verilog, Cadence

- EECS 251B Project: Worked alongside 17 other students to design IEEE Std 802.3 Ethernet 1000BASE-T IP
- Designed the TX Digital sub-module in RTL and ensured proper integration with other team's sub-modules
- Performed functional verification, synthesis, place-and-route, and timing closure using Cadence ASIC flow

RISC-V 3-Stage CPU Design | Verilog, Cadence

- EECS 251A ASIC Project: Designed and verified a 3-stage RISC-V processor in Verilog using ASIC industry tools
- Implemented support for 39 RV32I instructions and designed data-forwarding logic to resolve pipeline hazards
- Developed direct-mapped and 2-way set associative SRAM-based caches and the interface with main memory

CMOS Display Driver Design | Cadence Virtuoso

- EECS 240A Project: Designed a 2-stage op-amp display driver in 45nm CMOS, and met design requirements
- Sized the transistors using the gm/Id look-up method to meet small signal and DC operating conditions
- Simulated the DC and AC response of the circuit in Cadence Virtuoso using system-level testbenches

PCB Projects

Mixed-Signal Ultrasound Imager | UC Berkely Capstone Project | KiCad

- Designed a 6-layer mixed signal PCB for processing transmitting and receiving ultrasound signals
- Collaborated with algorithm developers to ensure signal integrity and targeted sampling frequency
- Selected components that fit full system requirements: VCA, ADCs, TR Switch, MCUs, Pulsers
- Implemented a power management system using LDOs, boosters, and inverters to generate required voltage levels
- Performed board bring-up and validated system functionality using oscilloscope, signal generator, and a multimeter

Smart Mezuzah Product | KiCad, Autodesk Fusion 360

- Accomplished first place in Jewish Engineering competition for creatively blending a ritual with engineering
- Designed an ultra low-power 1000mAh battery powered presence detection system that can last for up to 2 years
- Prototyped on a breadboard and designed a miniaturized PCB integrating energy harvesting and sensing electronics

IMU Maze Game | KiCad

- Created the game by integrating IMU for orientation, LCD for maze display, MCU, and haptic feedback

Hardware Work Experience

Rayne Research Group

Feb 2026 – May 2026

Graduate Student Researcher - PCB Designer

- Collaborated with Mechanical and Materials engineers to design a tactile sensing system for a robotic hand
- Integrated PZT sensors with a signal processing pipeline containing TIA, multiplexers, buffers, and an ADC
- Designed a flex-rigid miniaturized PCB for proper integration with robotic hand, and ensured signal integrity

Silicon Labs

May 2024 – Aug 2024

Applications Development Internship

Montreal, Canada

- Developed end-device applications using C++/C, Bash on various SoC architectures; enabling OTA & bootloader updates over the IEEE 802.15.4 Thread protocol, and documented the workflow for smooth customer adoption
- Implemented the first Matter Scenes Cluster application (CSA-IoT) and fully documented the methodology
- Built a Bash build automation script for streamlining SDK version switching, boosting team productivity

Matrox Imaging (now part of Zebra Technologies)

May 2022 – Aug 2022

RTL Design and Validation Internship

Montreal, Canada

- Implemented image-processing pipelines on Xilinx FPGAs using VHDL, contributing to the design of new frame-grabber designs in industrial inspection by adhering to the Camera Link protocol
- Engineered C++ automated test suites to probe image-acquisition edge cases, and verified with waveform analysis

The Heterogeneous Integration Knowledge Team

Jan 2022 – Apr 2022

Undergraduate Researcher

Montreal, Canada

- Researched floor planning algorithms to optimize thermal management in 3D integrated circuits
- Studied numerical methods, such as simulated annealing, to find local and global minima of a cost function
- Programmed in C++ to demonstrate how simulated annealing can be used for optimized parameter fine-tuning

Leadership

Semiconductor Affinity Group Leader | *Fung Institute, UC Berkeley*

Aug 2025 – May 2026

- Co-led the group, and planned events for students interested in the semiconductor industry

Teaching Assistant in Electronics | *McGill University*

Sep 2023 – Apr 2024

- Led weekly discussions, labs, and held office hours to support the learning of over 100 students in electronics

Finance Partner | *McGill Technical Sales Club*

Sep 2023 – Dec 2024

- Managed the club's budget to ensure efficient allocation of funds for student events.