EE 240A – Analog Integrated Circuits
UC Berkeley

Final Project

Design of a Display Driver

Completed by:

Tofic Esses
3041981205

Host: ee140-adn
Tools: Cadence Virtuoso

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1 Overview

1.1 Complete Schematic and Basic Circuit Description

The amplifier is made up of multiple building blocks: 1) Current source, 2) Telescopic Cascode Differential Amplifier with 3) its VBX Biasing network, 4) a Source Follower (which provides buffering to maintain output resistance), 5) a Class AB Output Stage biased with Monticello for device variability matching. The schematic can be seen in Fig. 3. NMOS based current mirrors are used to sink the necessary current through each stage.

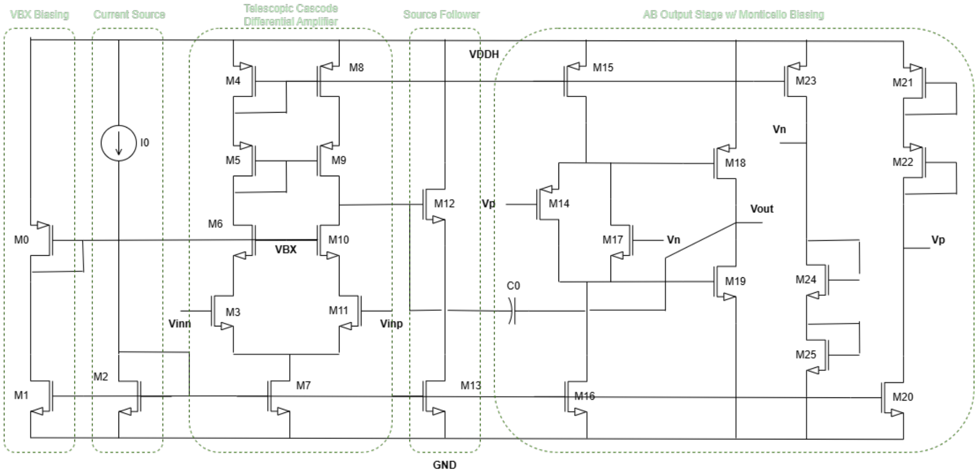


Figure 1: Amplifier Schematic

The schematic in Cadence Virtuoso can be seen in Fig. 2. Notice that only 2V devices were used because the source is VDDH. This prevents leakage current.

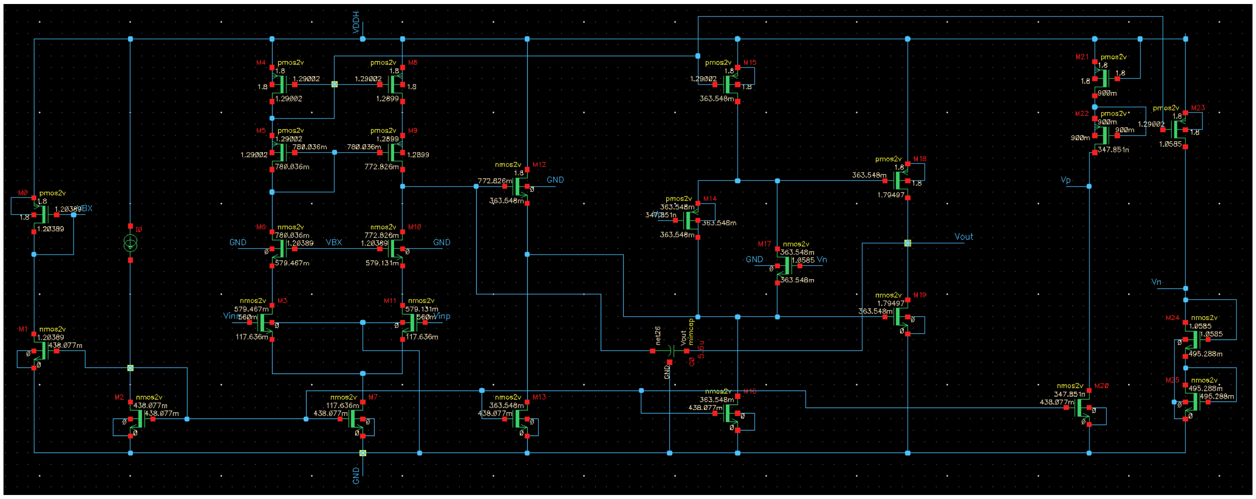


Figure 2: Cadence Amplifier Schematic

The final size of the transistors can be seen in Table 1 and Table 2. Table 3 shows the sizing for the Miller Capacitor, C0, which was minimized to bring the PM as close as possible to 45°.

Device Type	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12
Length (µm)	0.9	1	1	1	0.9	0.9	1	1	0.9	0.9	1	1	1
Width (µm)	1	10	30	40	10.79	10.79	6.16	80	10.79	10.79	6.16	40	50

Table 1: Transistor Sizing Table (M0–M12)

Device Type	M13	M14	M15	M16	M17	M18	M19	M20	M21	M22	M23	M24	M25
Length (µm)	1	0.15	0.9	1	0.15	0.9	0.15	1	0.15	0.15	1	0.15	0.15
Width (µm)	15	2.4	2.2	9	9.8	10.79	40	10	2.4	2.4	10	9.8	9.8

Table 2: Transistor Sizing Table (M13–M25)

Parameter	**Value**
Capacitance	37.576 fF
Width (µm)	5.6
Length (µm)	5.6
Multiplier	2
Total Capacitance	75.152 fF

Table 3: C0 Device Parameters

Parameter	**Value**
Bias Current (I_0)	10 µA

Table 4: Bias Current I_0 Used in the Design

1.2 Comparison to Design Specifications

The screenshots of the results can be found in the Appendix.

Specification	**EE 240A Requirement**	**Design @ 0.75 kΩ**	**Design @ 1 kΩ**	**Status**
Technology	Gpdk045	Gpdk045	Gpdk045	MET
Power Supplies	GND (0V), VDDL $\leq$ 1.1V, VDDH $\leq$ 1.8V	GND (0V), VDDH = 1.8V	GND (0V), VDDH = 1.8V	MET
Closed-Loop DC Gain	2	2	2	MET
Load	0.75–1 kΩ, 25 pF	0.75 kΩ, 25 pF	1 kΩ, 25 pF	MET
Settling Time (T_{settle})	For 1.4V step, rising and falling $\leq$ 180ns	rising 164ns, falling 132ns,	rising 177ns, falling 173ns	MET
Total Error	$\leq$ 0.2%	$\leq$ 0.2%	$\leq$ 0.2%	MET
Power Consumption	$\leq$ 0.75 mW	0.84 mW	0.90 mW	NOT MET
Output Voltage Swing	$\geq$ 1.4V	1.4V	1.4V	MET
Maximum Current Mirror Ratio	10	2.67 used	2.67 used	MET
Maximum Total Capacitance	5 pF	75.152 fF used	75.152 fF used	MET
Maximum Total Resistance	100 kΩ	0 Ω used	0 Ω used	MET
CMRR at DC	$\geq$ 55 dB	78.06 dB	78.06 dB	MET
PSRR at DC	$\geq$ 50 dB	68.33 dB	68.33 dB	MET
Phase Margin	$\geq 45^\circ$	47.94°.	48.45°.	MET
Figure of Merit (FoM)	$\frac{1}{T_{\text{settle}} \cdot P_{\text{total}}}$	9.42	6.874	N/A

Table 5: EE 240A Design Specifications and Verification for 0.75 kΩ and 1 kΩ Loads

2 Design

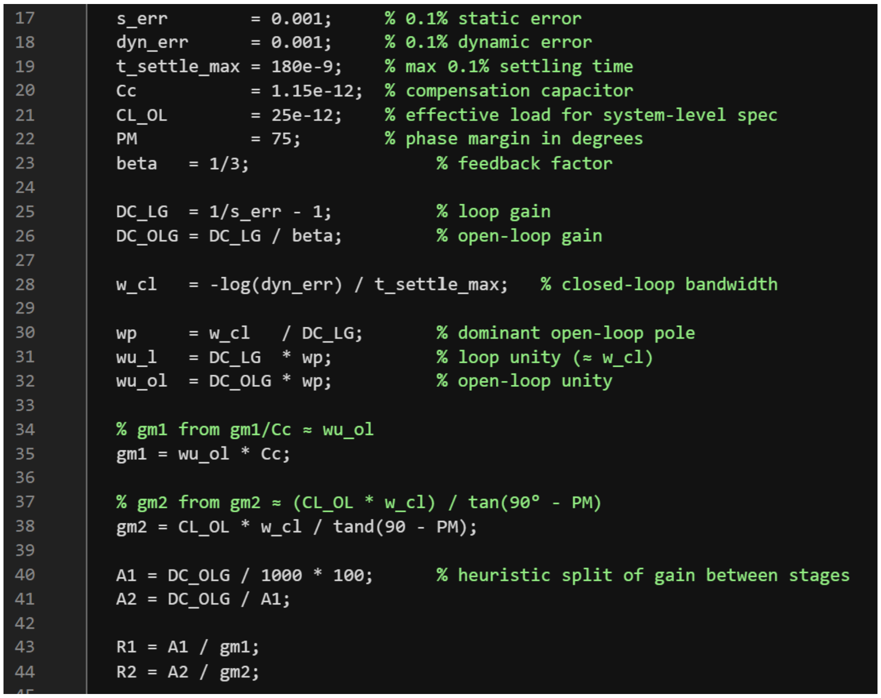
2.1 Design Approach and Amplifier-Level Specifications

In the initial phases of the design, the requirements were made clear in Week 1, Week 2, and Week 3 of the project timeline. Then it was up to Analog Designer (me) to choose a topology that satisfies all design requirements.

2.2 Key Design Equations and Sizing Methodology

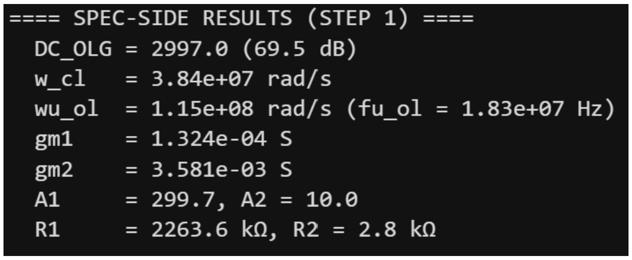
After finalizing the key design equations, constants, and parameters, a Matlab script was created for a quick and accurate generation of values.

The amplification of the first stage was decided to be 1000 V/V and the second stage 30 V/V.



```
s_err        = 0.001;     % 0.1% static error
dyn_err      = 0.001;     % 0.1% dynamic error
t_settle_max = 180e-9;    % max 0.1% settling time
Cc           = 1.15e-12;  % compensation capacitor
CL_OL        = 25e-12;    % effective load for system-level spec
PM           = 75;        % phase margin in degrees
beta   = 1/3;                  % feedback factor

DC_LG  = 1/s_err - 1;          % loop gain
DC_OLG = DC_LG / beta;         % open-loop gain

w_cl   = -log(dyn_err) / t_settle_max;   % closed-loop bandwidth

wp     = w_cl   / DC_LG;       % dominant open-loop pole
wu_l   = DC_LG  * wp;          % loop unity (≈ w_cl)
wu_ol  = DC_OLG * wp;          % open-loop unity

% gm1 from gm1/Cc ≈ wu_ol
gm1 = wu_ol * Cc;

% gm2 from gm2 ≈ (CL_OL * w_cl) / tan(90° - PM)
gm2 = CL_OL * w_cl / tand(90 - PM);

A1 = DC_OLG / 1000 * 100;      % heuristic split of gain between stages
A2 = DC_OLG / A1;

R1 = A1 / gm1;
R2 = A2 / gm2;
```

Figure 3: Matlab System Level Design Script



```
==== SPEC-SIDE RESULTS (STEP 1) ====
  DC_OLG = 2997.0 (69.5 dB)
  w_cl   = 3.84e+07 rad/s
  wu_ol  = 1.15e+08 rad/s (fu_ol = 1.83e+07 Hz)
  gm1    = 1.324e-04 S
  gm2    = 3.581e-03 S
  A1     = 299.7, A2 = 10.0
  R1     = 2263.6 kΩ, R2 = 2.8 kΩ
```

Figure 4: Matlab Output

After generating gm1 and gm2 from the Matlab script, the gmId sizing script was used to size W and L.

These sizes were used as an initial starting point. After running the simulation for the first time with all bias points and sizes set, it was noted that the simulation did not perform as expected.

The way to overcome this hurdle was to inspect the DC operating conditions of each transistor and to ensure they are where they should be.

To adjust discrepancies, sweeping W, L, bias current, and bias voltage was used. This was, of course, time consuming process.

2.3 Topology Decisions

- **Telescopic Cascoded Differential Amplifier:** Increase output resistance, to increase the gain.
- **Source Follower:** Create a large input impedence seen by the first stage to avoid signal attentuation.
- **AB Output Stage:** NMOS and PMOS Source followers to produce gain, biased by Monticello to reduce quiescent current consumption, effectively reducing power.

2.4 Discussion for Variability and Mismatch

During chip fabrication, inevitable variations in device dimensions and process parameters can cause transistor mismatches that shift bias currents and operating points in sensitive analog circuits. To ensure robustness against these effects, the Monticello Biasing Network was deliberately chosen, as its symmetric structure and built-in local feedback help stabilize bias currents and reduce sensitivity to threshold voltage and mobility variations. This improves the amplifier's resilience to mismatch, particularly in the second stage, and ensures more consistent performance across process and temperature variations.

3 Transistor and Bias Summary

3.1 Operating Point Summary Table

Device	—ID— (A)	—VGS— (V)	gm (S)
M0	3.90022u	0.596108	40.0333u
M1	3.90029u	0.438077	73.9329u
M2	10u	0.438077	196.225u
M3	10.6297u	0.442364	216u
M4	10.6279u	0.509979	194.33u
M5	10.6289u	0.509984	194.342u
M6	10.6297u	0.634425	146.515u
M7	21.2576u	0.438077	429.541u
M8	10.6283u	0.509979	194.335u
M9	10.6279u	0.509862	194.354u
M10	10.6279u	0.579131	146.227u
M11	10.6279u	0.442364	215.967u
M12	4.17203u	0.648028	98.2668u
M13	4.67892u	0.438077	92.5719u
M14	3.64989p	0.363548	0
M15	3.07673u	0.509979	51.937u
M16	2.60311u	0.438077	51.8691u
M17	155.436n	0.66321	0
M18	6.30611u	1.43645	2.64231u
M19	6.30611u	1.43645	165.823u
M20	21.4891p	0.438077	356.75p
M21	12.5893p	0.963202m	23.9269p
M22	12.5893p	0.963202m	23.9269p
M23	10.6692u	0.509979	189.361u
M24	10.6692u	0.56321	209.736u
M25	10.6692u	0.495288	208.859u

Table 6: Transistor and Bias Summary

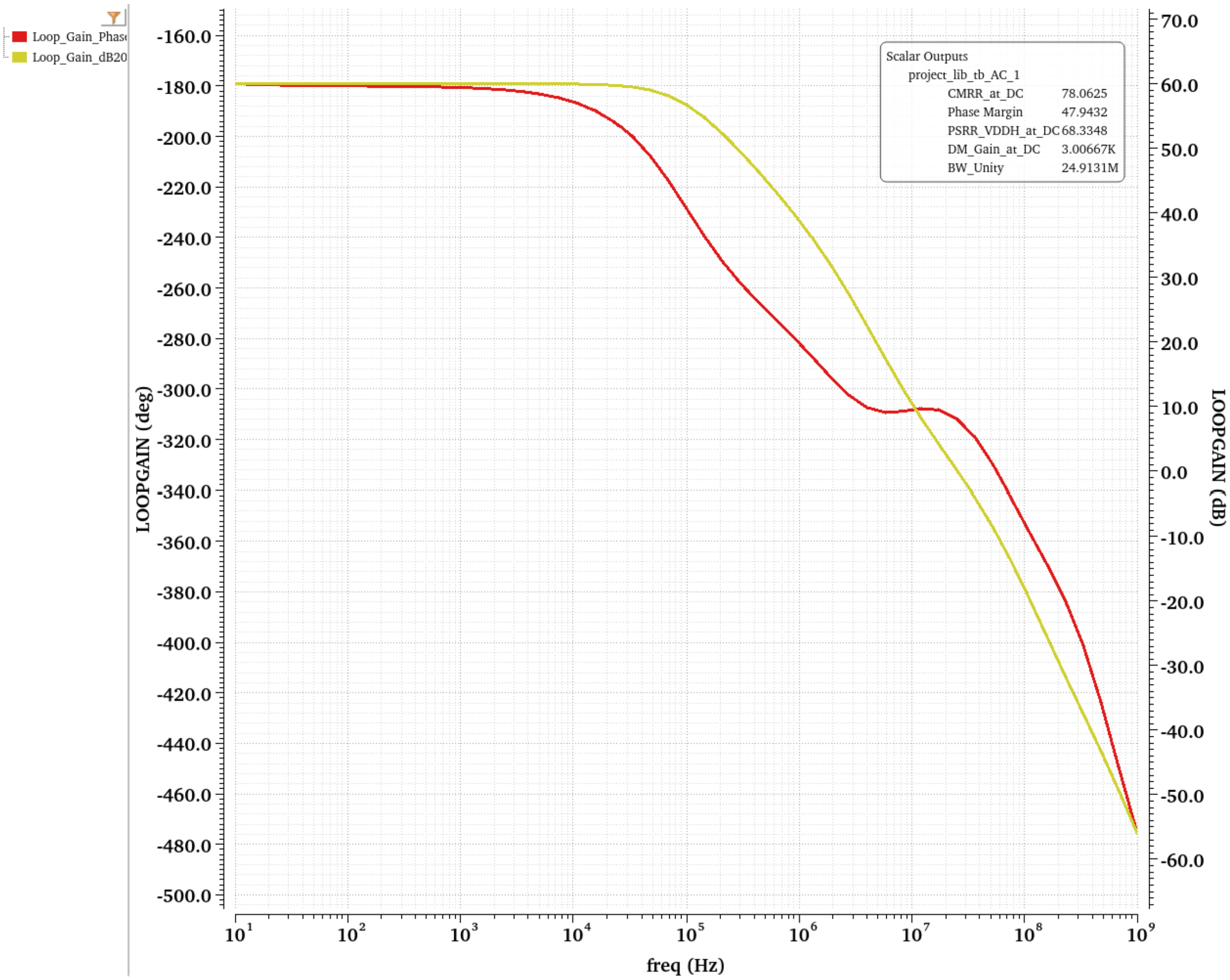
4 Discussion

Below contains all the simulated results.

4.1 AC Performance

4.1.1 Loop Gain Bode Plot, Mid-Band Gain, and Phase Margin

i. 0.75 kΩ



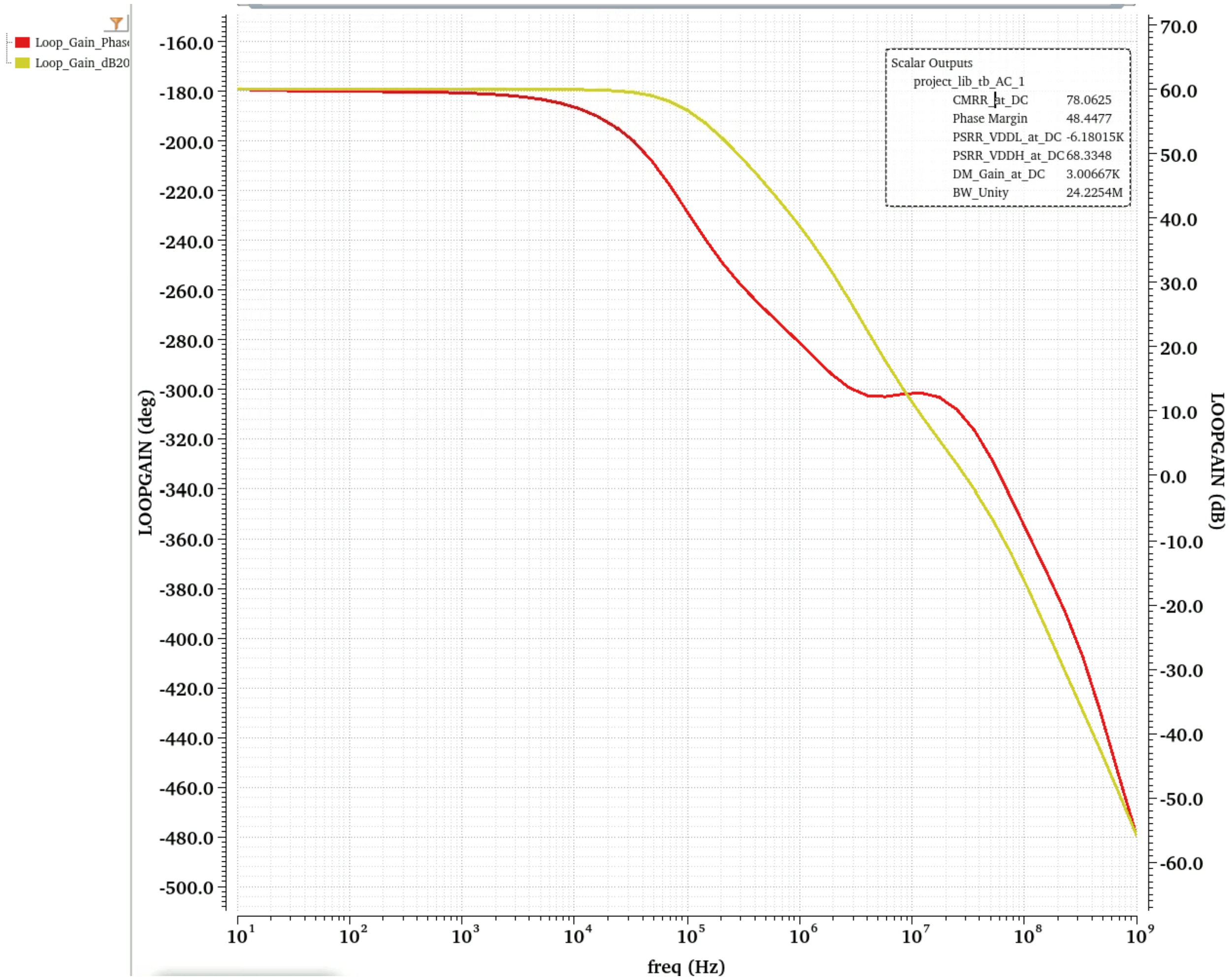
Scalar Outputs

project_lib_tb_AC_1

CMRR_at_DC	78.0625
Phase Margin	47.9432
PSRR_VDDH_at_DC	68.3348
DM_Gain_at_DC	3.00667K
BW_Unity	24.9131M

Figure 5: 0.75 kΩ Loop Gain & Loop Plot

ii. 1 kΩ



```
Scalar Outputs
    project_lib_tb_AC_1
        CMRR_at_DC          78.0625
        Phase Margin        48.4477
        PSRR_VDDL_at_DC -6.18015K
        PSRR_VDDH_at_DC68.3348
        DM_Gain_at_DC       3.00667K
        BW_Unity            24.2254M
```

Figure 6: 1 kΩ Loop Gain & Loop Plot

4.1.2 CMG & CMRR vs Frequency

i. 0.75 kΩ

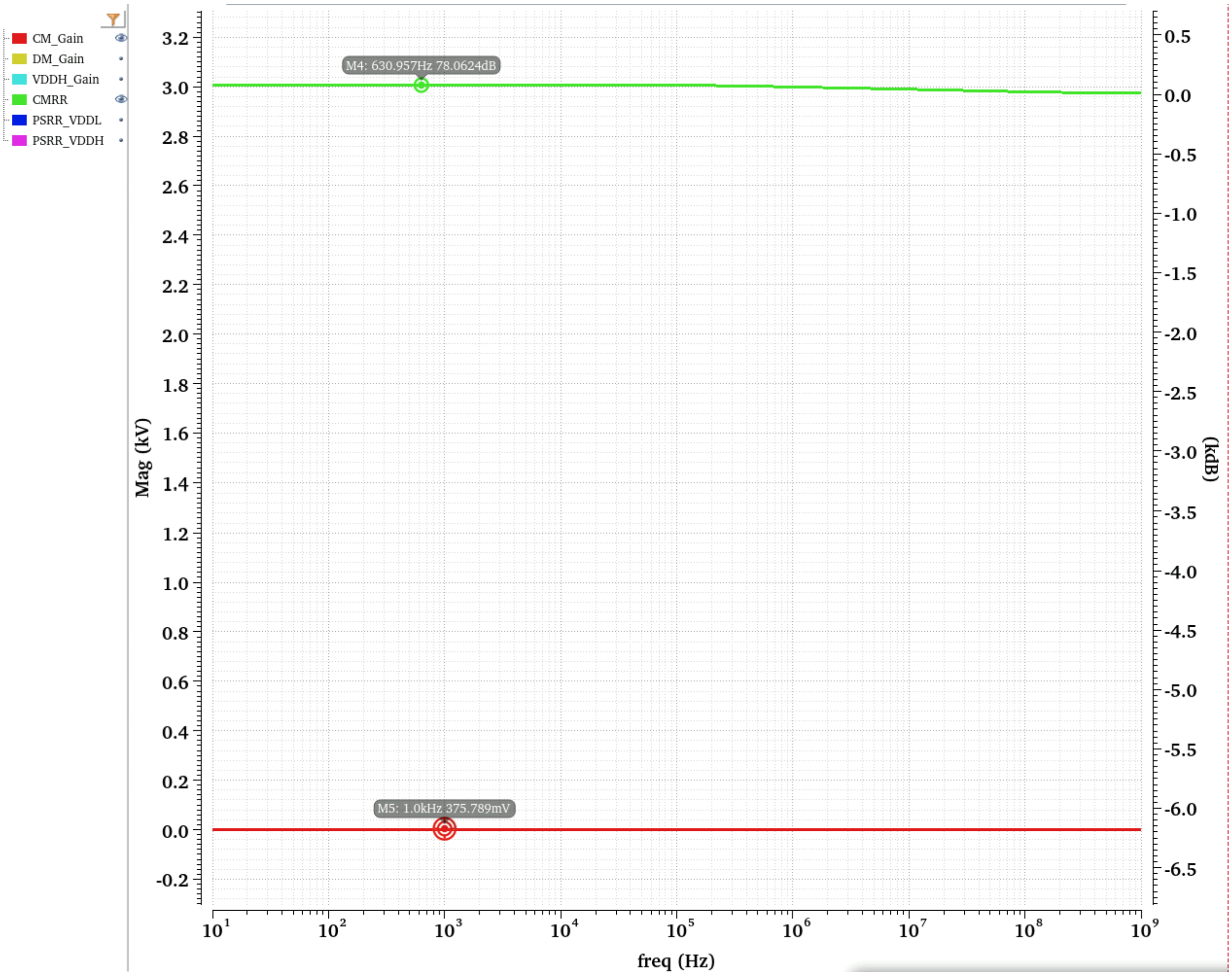


Figure 7: 0.75 kΩ CMG & CMRR vs Frequency

ii. 1 kΩ

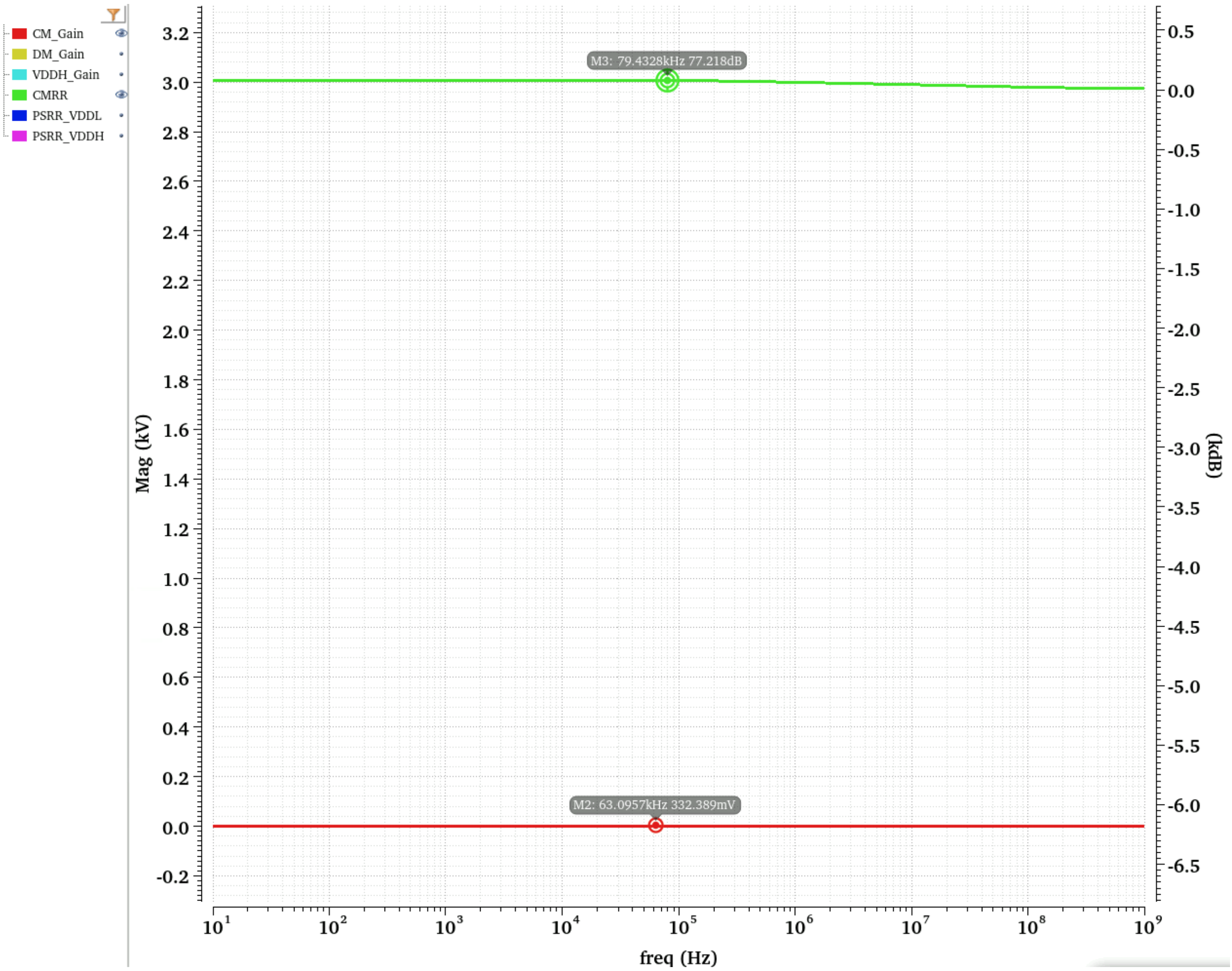


Figure 8: 1 kΩ CMG & CMRR vs Frequency

4.1.3 VDDH Gain & PSSR vs Frequency

i. 0.75 kΩ

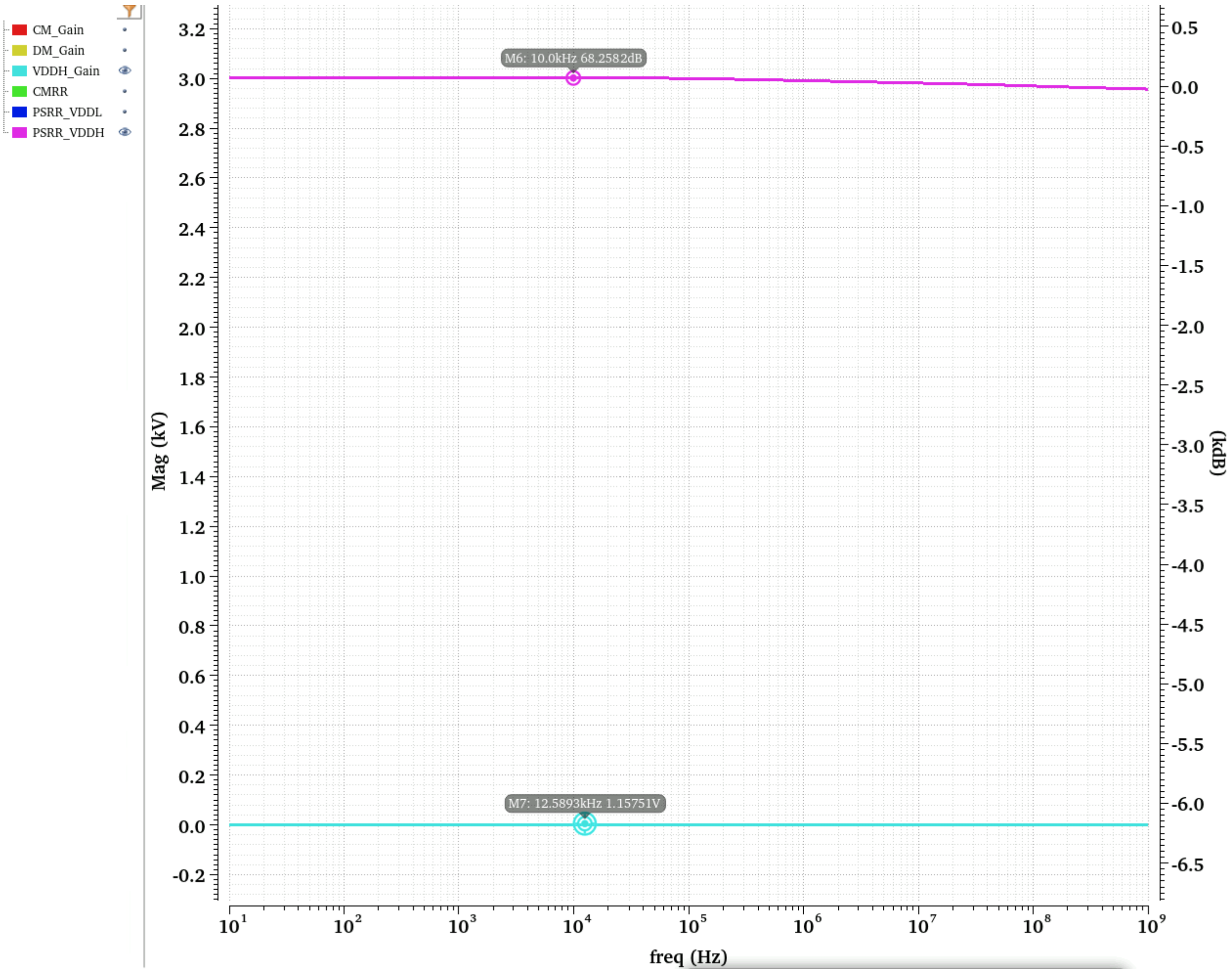


Figure 9: 0.75 kΩ VDDH & PSSR vs Frequency

ii. 1 kΩ

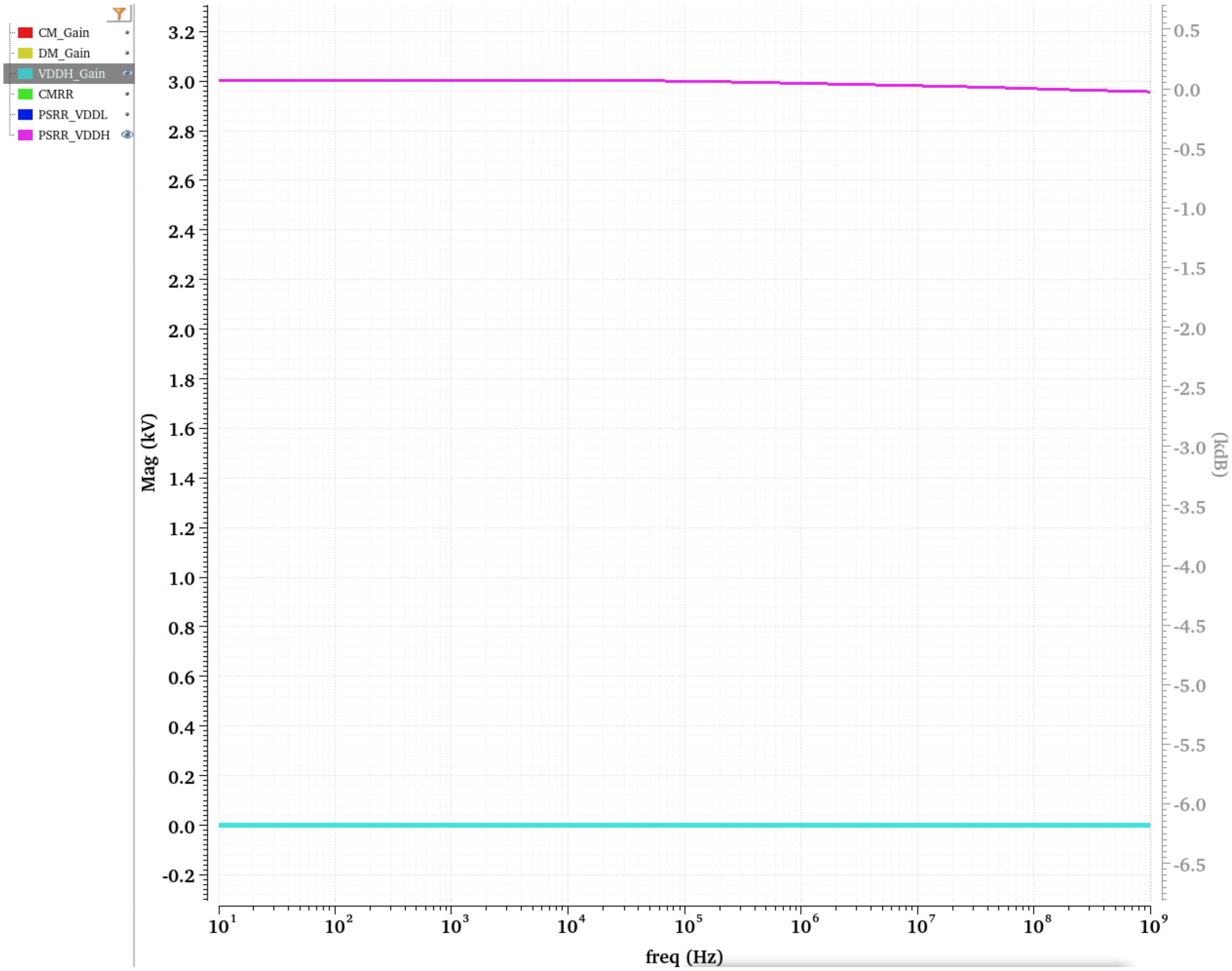


Figure 10: 1 kΩ VDDH & PSSR vs Frequency

4.1.4 Load Dependence 0.75 kΩvs 1 kΩ

There is no major noticable difference. The system is stable for these two loads.

4.2 Transient Performance

4.2.1 Load Capacitor Output Waveforms

Based on the plots below, it is clear to say that the amplification due to the input is equal to 2V/V. This requirement is met!

ii. 0.75 kΩ

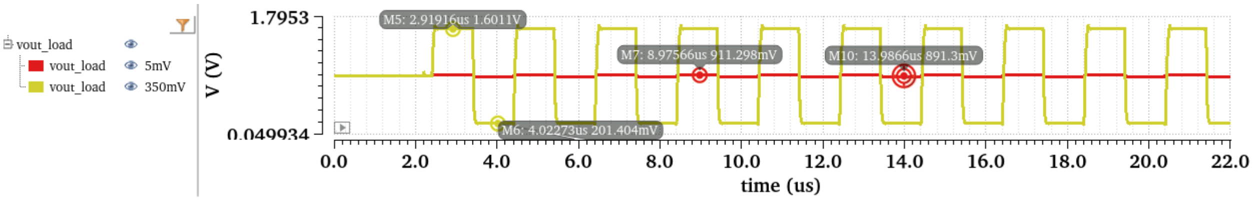


Figure 11: 0.75 kΩ Load Capacitor Output Waveform

ii. 1 kΩ

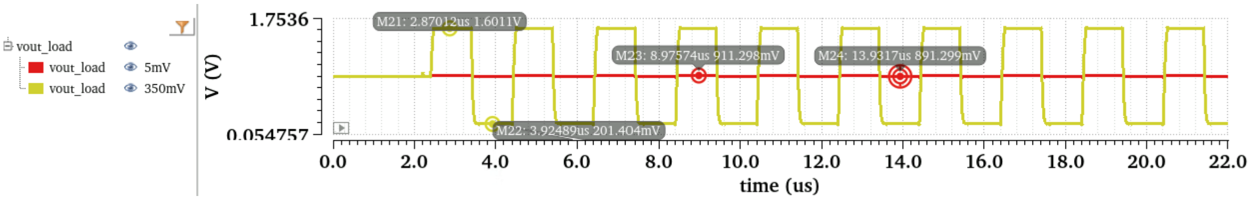


Figure 12: 1 kΩ Load Capacitor Output Waveform

ii. 0.75 kΩ

In both cases below, the settling error is reached before the max settling time.

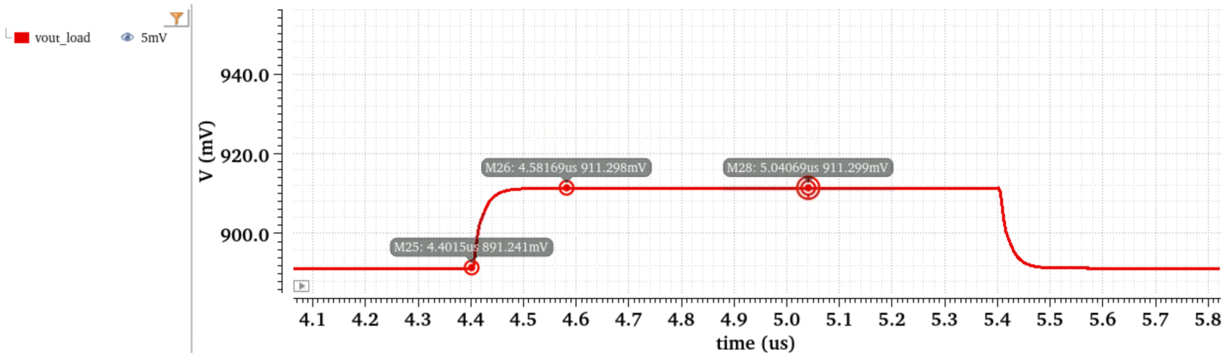


Figure 13: 075 kΩ Load Capacitor Output Settle with 5mV

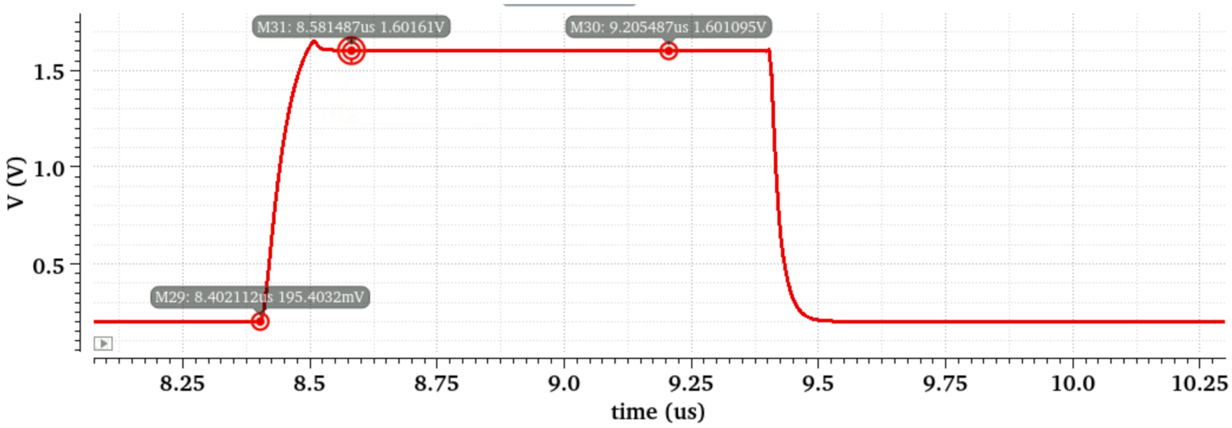


Figure 14: 075 kΩ Load Capacitor Output Settle with 350mV

ii. 1 kΩ

In both cases below, the settling error is reached before the max settling time.

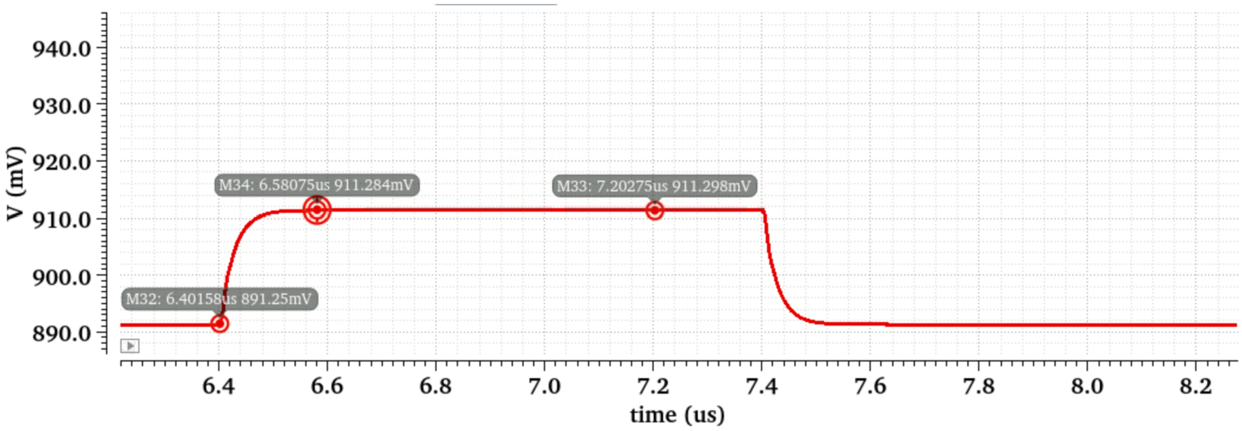


Figure 15: 1 kΩ Load Capacitor Output Settle with 5mV

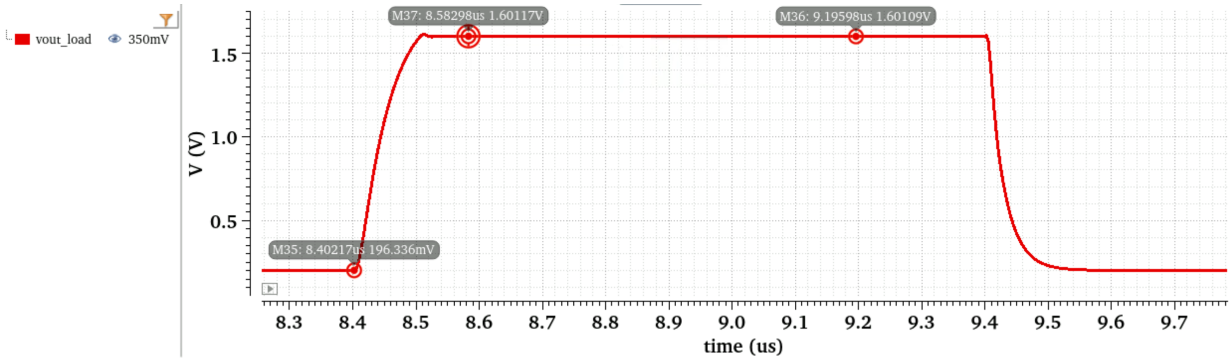


Figure 16: 1 kΩ Load Capacitor Output Settle with 350mV

4.2.2 Amplifier Output Waveforms

The amplifier output closely resembles the capacitive loaded output, as expected.

ii. 0.75 kΩ

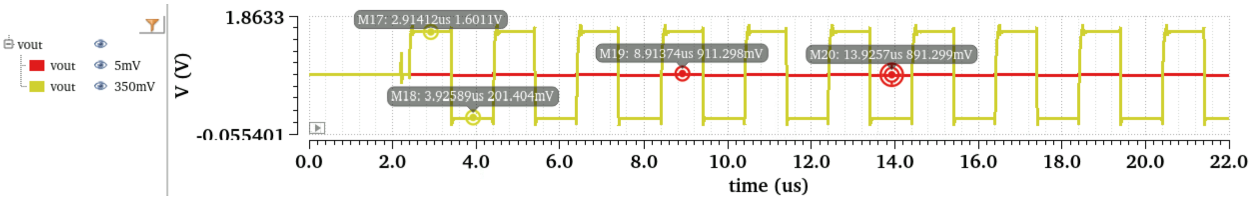


Figure 17: 0.75 kΩ Amplifier Output Waveform

ii. 1 kΩ

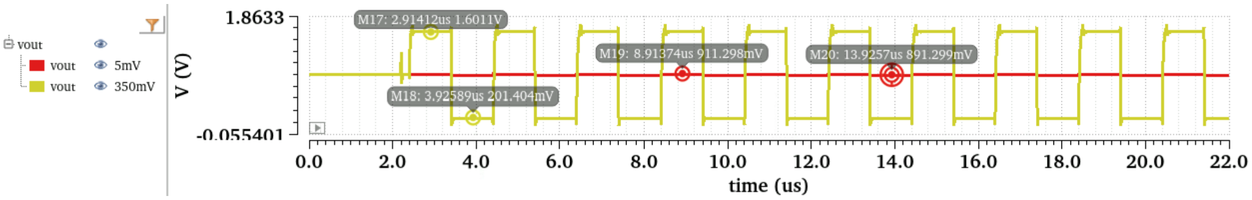


Figure 18: 1 kΩ Amplifier Output Waveform

4.2.3 Settling Error for Output Steps

In all cases, the error settles quickly, and from Maestro, it shows that the settling time is below 180ns. So the error is below the maximum error.

ii. 0.75 kΩ

project_lib_tb_tr...	fall_time				128.7n	131.9n	128.7n	131.9n
project_lib_tb_tr...	settle_time				128.8n	164.2n	128.8n	164.2n

Figure 19: 0.75 kΩ Fall and Settle time

ii. 1 kΩ

project_lib_tb_tr...	fall_time				173.2n	176.9n	173.2n	176.9n
project_lib_tb_tr...	settle_time				173.3n	176.9n	173.3n	176.9n

Figure 20: 1 kΩ Fall and Settle time

ii. 0.75 kΩ

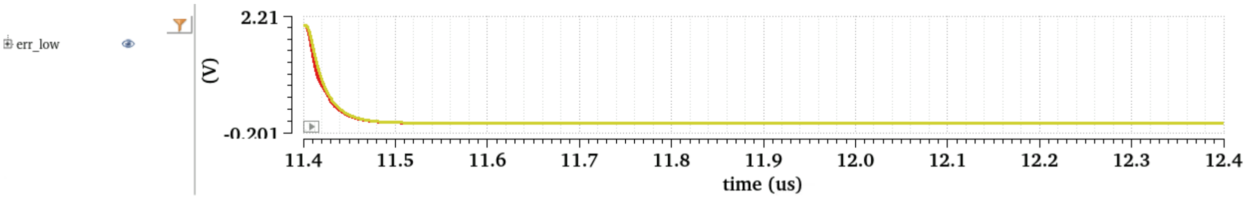


Figure 21: 0.75 kΩ Error Low

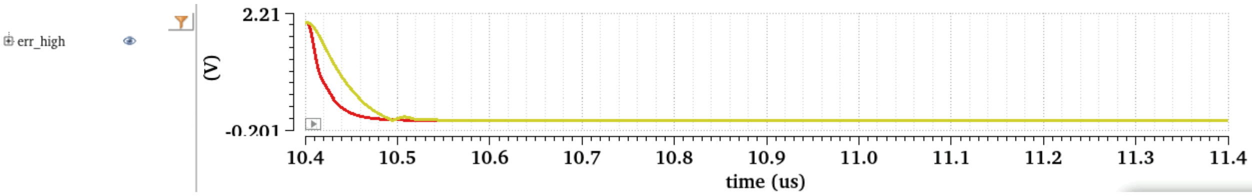


Figure 22: 0.75 kΩ Error High

ii. 1 kΩ

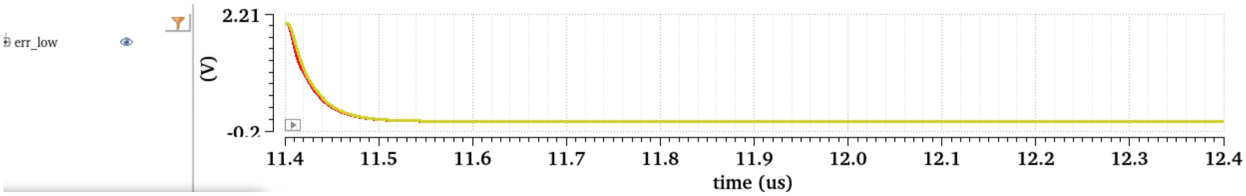


Figure 23: 1 kΩ Error Low

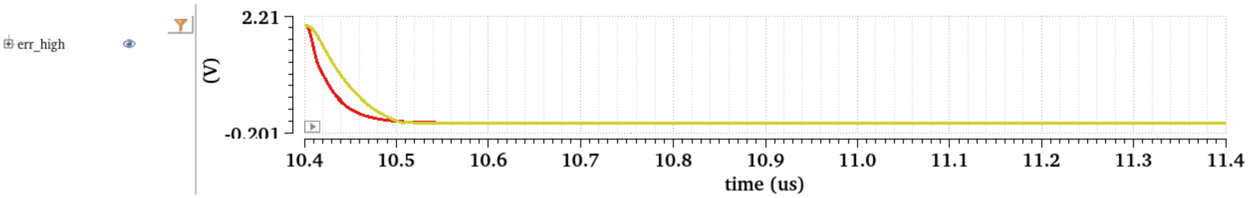


Figure 24: 1 kΩ Error High

4.2.4 Supply Currents from VDDH

The supply current is high before each switch because there is a sudden transition. Once the capacitor charges/discharges, the current stabilizes.

ii. 0.75 kΩ

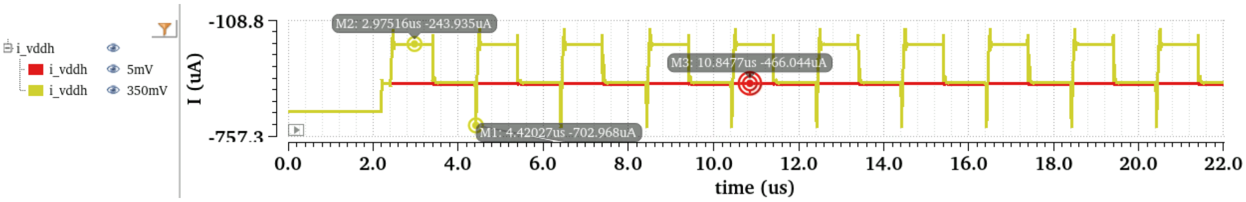


Figure 25: 0.75 kΩ Supply Current

ii. 1 kΩ

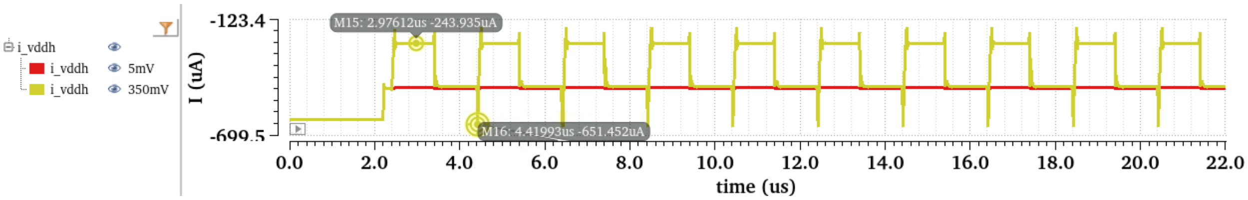


Figure 26: 1 kΩ Supply Current

4.2.5 Load Dependence 750 Ω vs 1 kΩ

A larger load takes more time for the voltage to fall/settle, because the RC constant at the output is larger.

4.3 Testbench Setup

See Fig. 27 for the transient testbench (one of the many testbenches) set up. The load resistance RL is set as a variable so that it is simple to test under a 0.75 kΩ and 1 kΩ load resistance.

The capacitors in the feedback loop were adjusted to match the setup of the display driver in Fig. 28.

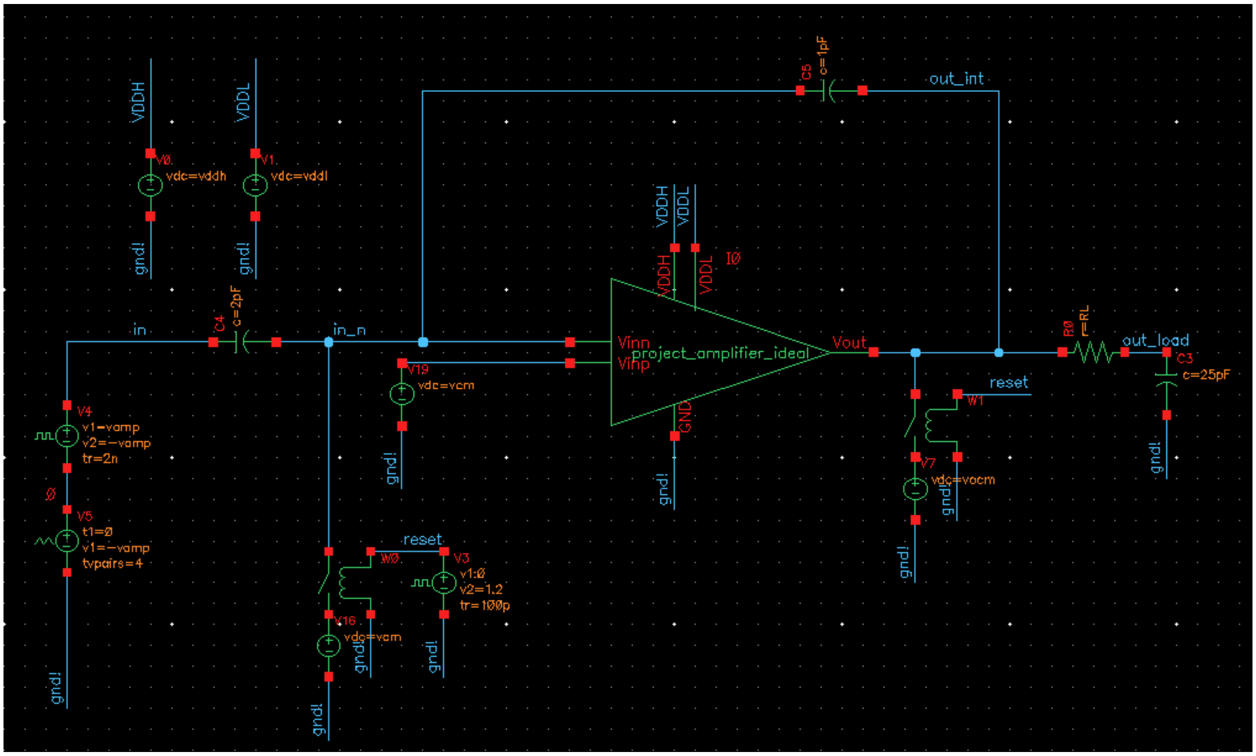


Figure 27: Transient Testbench Schematic

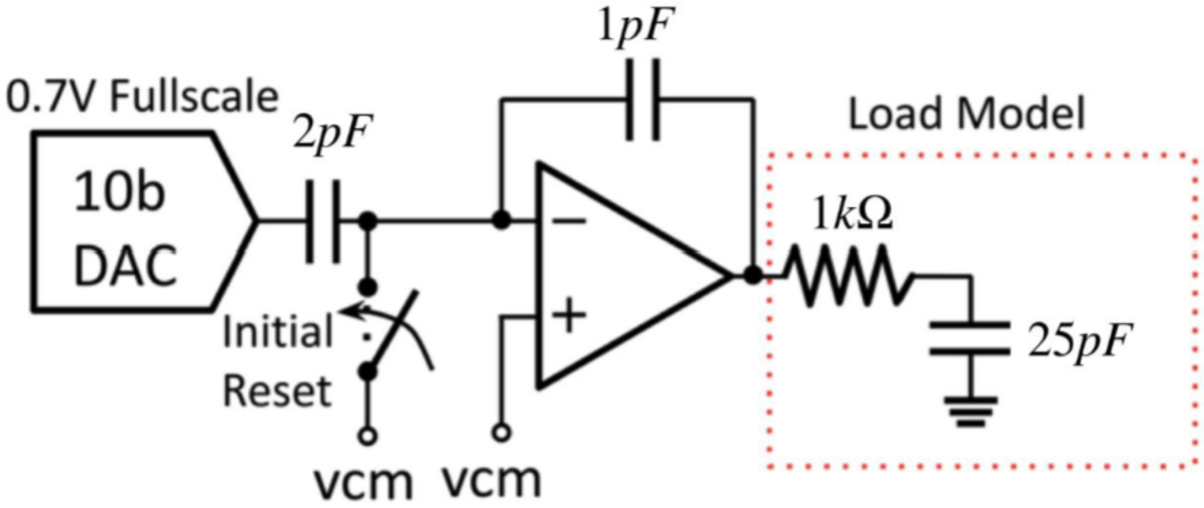


Figure 28: Driver Schematic

4.4 Area Estimation

Based on Tables 1, 2, 3, the total area is estimated to be:

$$\boxed{A_{\text{total}} = 431.965\ \mu\text{m}^2}$$

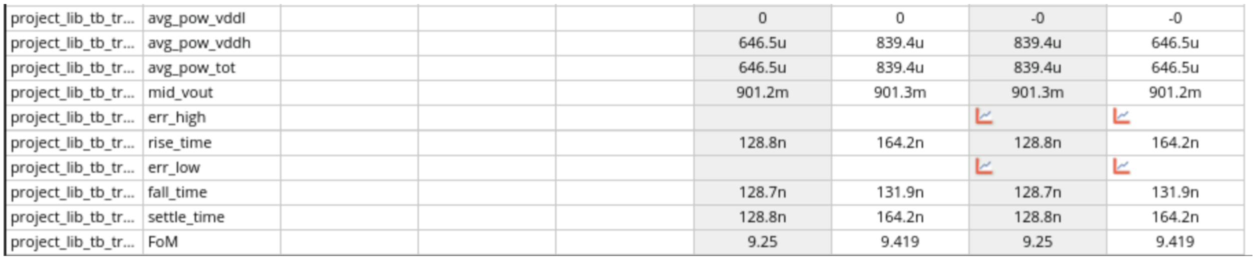
5 Conclusion

5.1 Summary of Op Amp Characteristics

In summary, most specifications were successfully met, with the exception of the maximum power requirement. While the design satisfies the looser power constraint used in EE140, it does not meet the stricter EE240A limit. With additional time, I would further refine the biasing network and reduce the sizing of the bias current sinks to lower the overall quiescent current. These modifications would meaningfully reduce power consumption, and I am confident that, with continued iteration, the amplifier could meet the EE240A power specification as well.

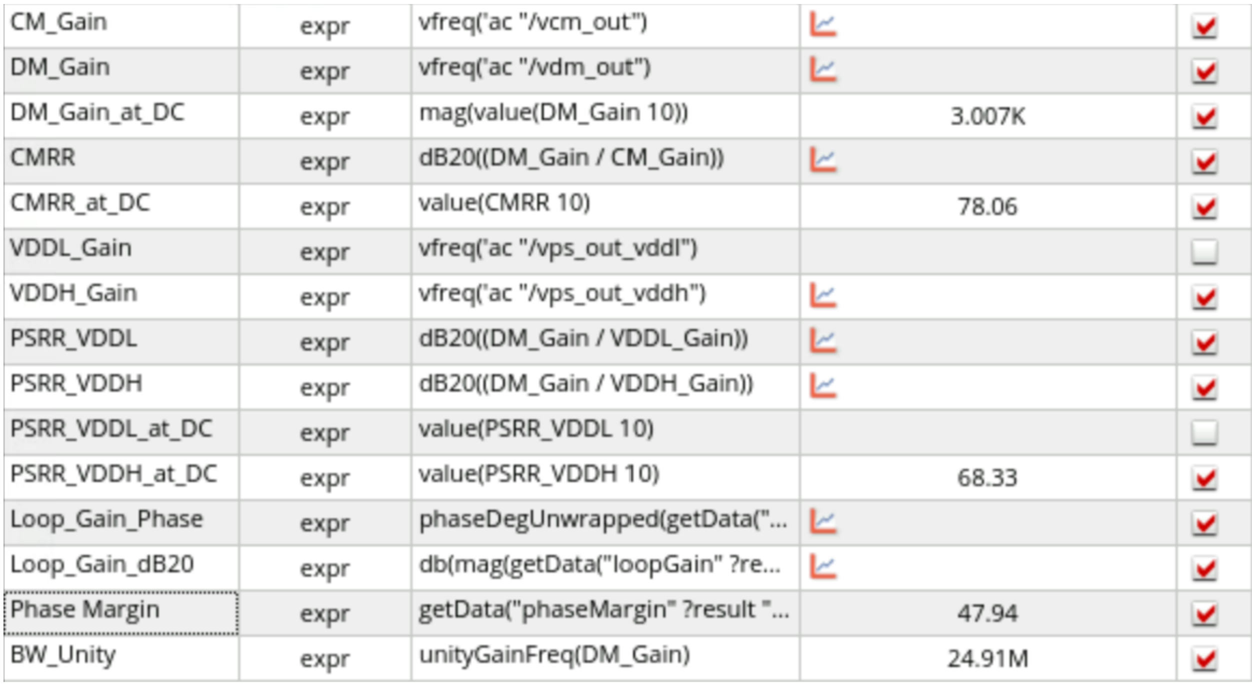
6 Appendix: Proof of Design Met

6.0.1 0.75 kΩ Results



project_lib_tb_tr...	avg_pow_vddl				0	0	-0	-0
project_lib_tb_tr...	avg_pow_vddh				646.5u	839.4u	839.4u	646.5u
project_lib_tb_tr...	avg_pow_tot				646.5u	839.4u	839.4u	646.5u
project_lib_tb_tr...	mid_vout				901.2m	901.3m	901.3m	901.2m
project_lib_tb_tr...	err_high						📈	📈
project_lib_tb_tr...	rise_time				128.8n	164.2n	128.8n	164.2n
project_lib_tb_tr...	err_low						📈	📈
project_lib_tb_tr...	fall_time				128.7n	131.9n	128.7n	131.9n
project_lib_tb_tr...	settle_time				128.8n	164.2n	128.8n	164.2n
project_lib_tb_tr...	FoM				9.25	9.419	9.25	9.419

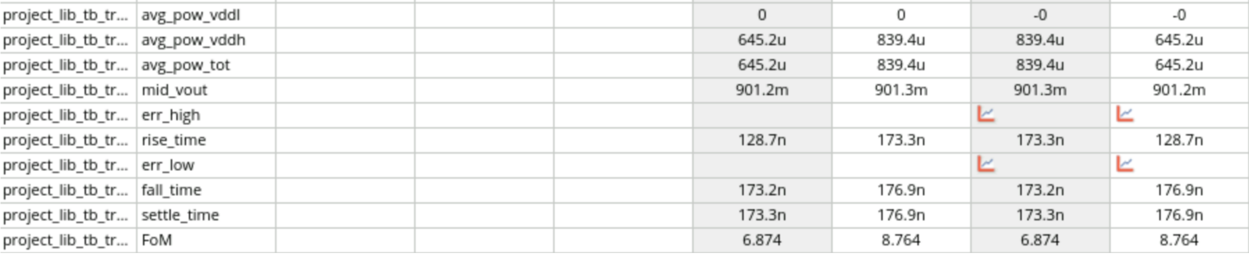
Figure 29: Transient 0.75 kΩ Results



CM_Gain	expr	vfreq('ac "/vcm_out")	📈	☑
DM_Gain	expr	vfreq('ac "/vdm_out")	📈	☑
DM_Gain_at_DC	expr	mag(value(DM_Gain 10))	3.007K	☑
CMRR	expr	dB20((DM_Gain / CM_Gain))	📈	☑
CMRR_at_DC	expr	value(CMRR 10)	78.06	☑
VDDL_Gain	expr	vfreq('ac "/vps_out_vddl")		☐
VDDH_Gain	expr	vfreq('ac "/vps_out_vddh")	📈	☑
PSRR_VDDL	expr	dB20((DM_Gain / VDDL_Gain))	📈	☑
PSRR_VDDH	expr	dB20((DM_Gain / VDDH_Gain))	📈	☑
PSRR_VDDL_at_DC	expr	value(PSRR_VDDL 10)		☐
PSRR_VDDH_at_DC	expr	value(PSRR_VDDH 10)	68.33	☑
Loop_Gain_Phase	expr	phaseDegUnwrapped(getData("...	📈	☑
Loop_Gain_dB20	expr	db(mag(getData("loopGain" ?re...	📈	☑
Phase Margin	expr	getData("phaseMargin" ?result "...	47.94	☑
BW_Unity	expr	unityGainFreq(DM_Gain)	24.91M	☑

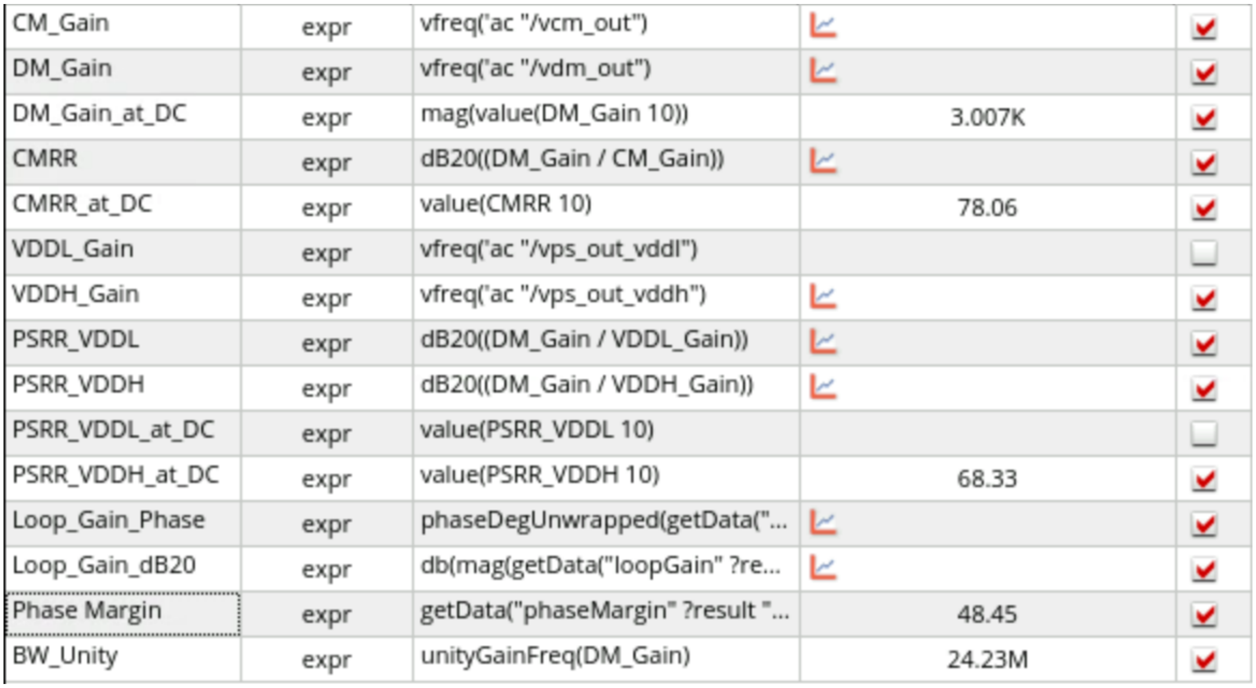
Figure 30: AC 0.75 kΩ Results

6.0.2 1 kΩ Results



project_lib_tb_tr...	avg_pow_vddl				0	0	-0	-0
project_lib_tb_tr...	avg_pow_vddh				645.2u	839.4u	839.4u	645.2u
project_lib_tb_tr...	avg_pow_tot				645.2u	839.4u	839.4u	645.2u
project_lib_tb_tr...	mid_vout				901.2m	901.3m	901.3m	901.2m
project_lib_tb_tr...	err_high						📈	📈
project_lib_tb_tr...	rise_time				128.7n	173.3n	173.3n	128.7n
project_lib_tb_tr...	err_low						📈	📈
project_lib_tb_tr...	fall_time				173.2n	176.9n	173.2n	176.9n
project_lib_tb_tr...	settle_time				173.3n	176.9n	173.3n	176.9n
project_lib_tb_tr...	FoM				6.874	8.764	6.874	8.764

Figure 31: Transient 1 kΩ Results



CM_Gain	expr	vfreq('ac "/vcm_out")	📈	☑
DM_Gain	expr	vfreq('ac "/vdm_out")	📈	☑
DM_Gain_at_DC	expr	mag(value(DM_Gain 10))	3.007K	☑
CMRR	expr	dB20((DM_Gain / CM_Gain))	📈	☑
CMRR_at_DC	expr	value(CMRR 10)	78.06	☑
VDDL_Gain	expr	vfreq('ac "/vps_out_vddl")		☐
VDDH_Gain	expr	vfreq('ac "/vps_out_vddh")	📈	☑
PSRR_VDDL	expr	dB20((DM_Gain / VDDL_Gain))	📈	☑
PSRR_VDDH	expr	dB20((DM_Gain / VDDH_Gain))	📈	☑
PSRR_VDDL_at_DC	expr	value(PSRR_VDDL 10)		☐
PSRR_VDDH_at_DC	expr	value(PSRR_VDDH 10)	68.33	☑
Loop_Gain_Phase	expr	phaseDegUnwrapped(getData("...	📈	☑
Loop_Gain_dB20	expr	db(mag(getData("loopGain" ?re...	📈	☑
Phase Margin	expr	getData("phaseMargin" ?result "...	48.45	☑
BW_Unity	expr	unityGainFreq(DM_Gain)	24.23M	☑

Figure 32: AC 1 kΩ Results